**Analogue to Digital Conversion II**

**Uniform quantisation**

**Analogue to Digital Converter (ADC**)

ZOH = zero-order-hold

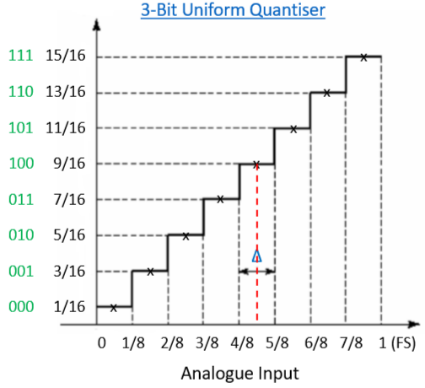
1. Anti-alias filter = removes **aliased** frequencies
2. ZOH(Sampling)**(1.1)** = holds input values until triggered

ADC diagram

1. Quantiser(Quantization)**(2.1)** = maps held input values to discrete value

**N-bit Uniform Quantisation**

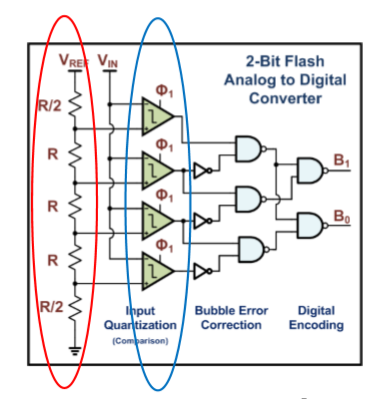
Voltage range = 2N Quantization step = Discrete voltage = (k+(k+1))Δ / 2

Voltage in interval [kΔ, (k+1)Δ], k=0,1,…, 2N-1 Max Quantisation error amplitude = Δ / 2

**Quantisation Error**

Relative max amplitude error = 2-(N+1)

Quantisation noise power = Δ2 / 12



**Flash and Sigma-Delta quantisers**

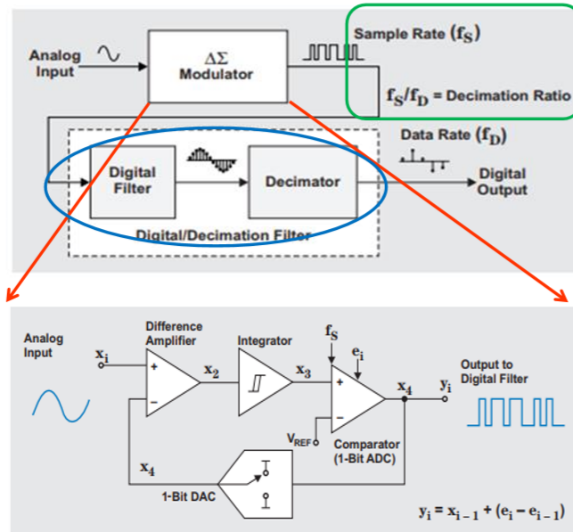
**Flash Quantiser**

* Use voltage ladder to generate successive reference voltages

Produce 2N quantization intervals simultaneously

* Use 2N comparators to find the quantisation interval the input VIN belongs to, in a single step
* Fastest, simple but could require a huge number of comparators

**Sigma-Delta Quantiser**

* Oversample the analog input
* Sigma-Delta modulator

The number of ‘ones’ in the modulator output is proportional to input value

* Digital/decimator accumulates modulator output over time

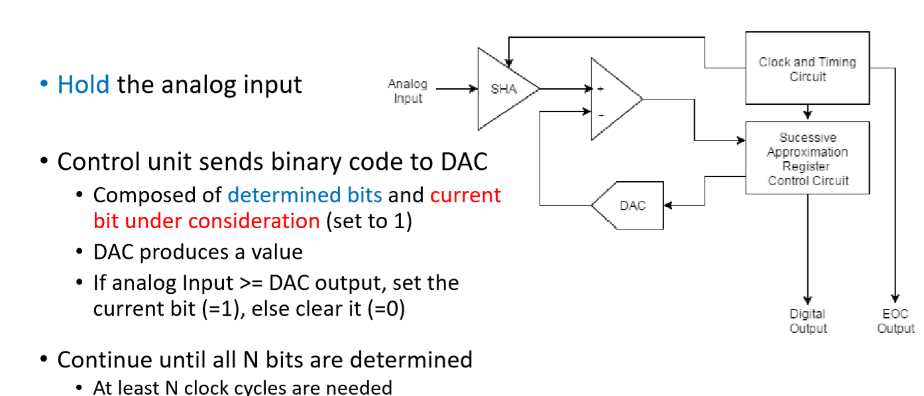
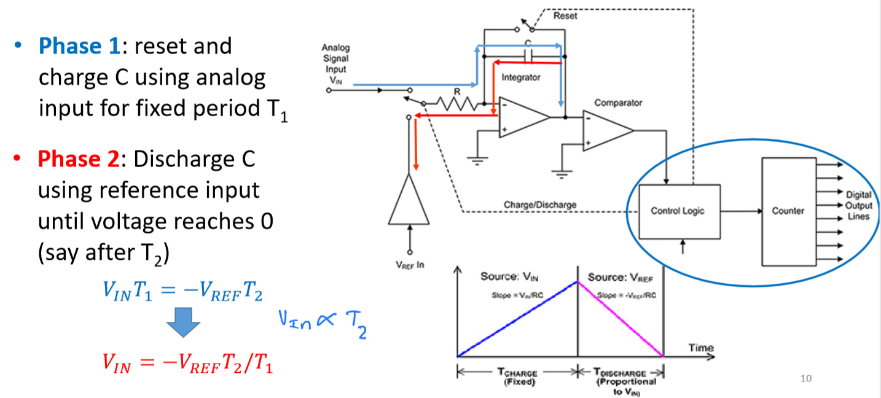
Output digital signals with required sampling rate

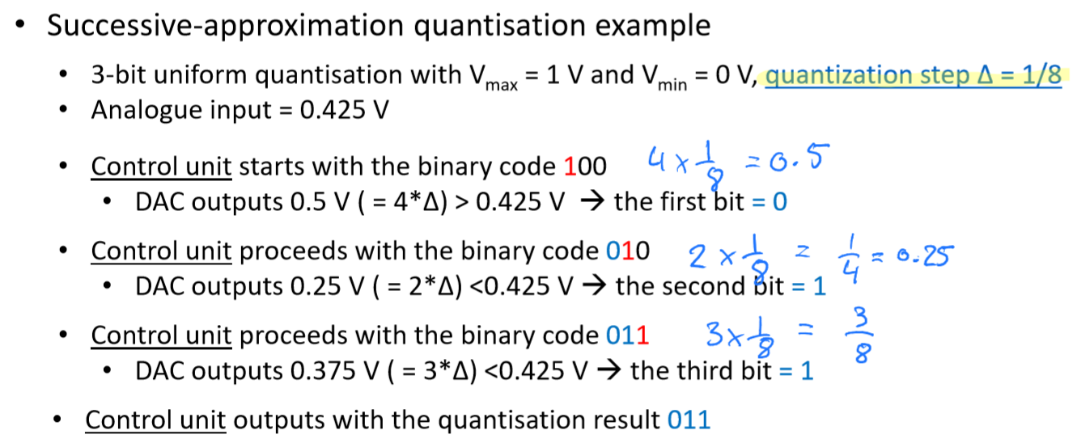
* High resolution, popular in communications engineering

**Dual-slop integrating and successive-approximation quantisers**

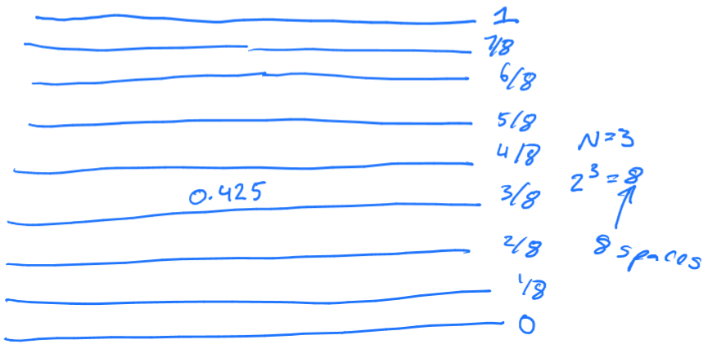
**Successive-Approximation Quantiser**

**Dual-Slope Integrating Quantiser**

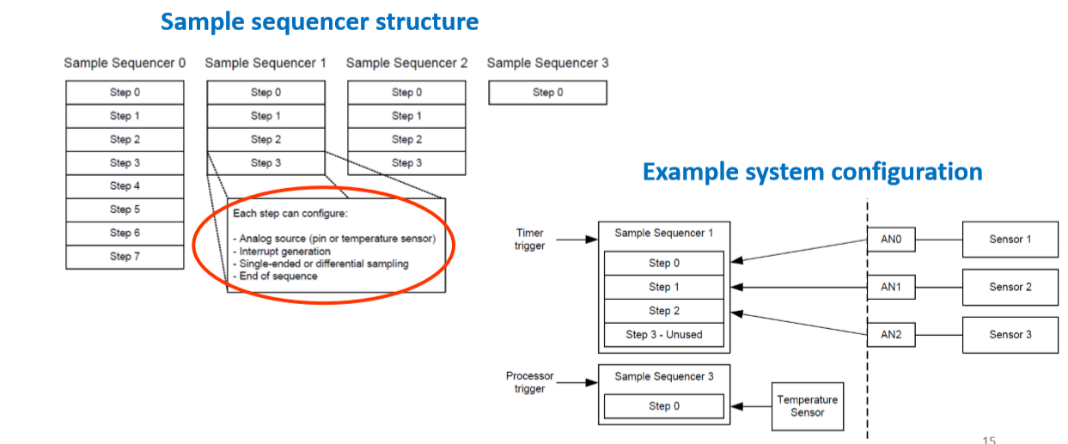


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Example

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* If analog Input >= DAC output, set the current bit (=1), else clear it (=0)



**12-bit ADC Module**

* 2 ADC modules

Each have = 4 sample sequencers - Each sequencer with configurable trigger - Each sequencer has 1, 4 or 8 steps

* 8 input channels and an internal temperature sensor.

What Quantiser does the Tiva board use = Successive-approximation based ADC